Implementation of a Distribution Static Compensator D-STATCOM: Hardware and Firmware Description

Implementación de un compensador estático de reactivos en distribución D-STATCOM: Descripción del Hardware y Firmware

S. Benavides-Córdoba ; J.R. Ortiz-Castrillón ; N. Muñoz-Galeano ; J.B. Cano-Quintero ; J.M. López-Lezama

***Abstract*—Distribution Static Power Compensator (D-STATCOM) is a device for reactive power compensation in electric distribution networks that presents advantages over conventional capacitors since it avoids power resonances and can perform a continuous compensation reaching a power factor near to unity. This paper describes the implementation of a D-STATCOM for reactive compensation in electric distribution networks, making a rigorous explanation of each component. A three-phase inverter of six pulses with two levels was developed. Hardware implementation of different stages (sensors, power switching, passive elements, and processor) is fully described. Firmware that allows D-STATCOM operation was implemented on a TMS3202F DSP (Texas Instruments) using a modular approach. Correct operation of the D-STATCOM prototype is verified with experimental results. Results showed appropriate power factor correction, reduction in the current demanded to the electrical grid and correct behavior of the control system, algorithms and hardware.**

***Index Terms*— Digital processing, DSP, D-STATCOM, microcontroller, power electronics.**

***Resumen*— El compensador estático de potencia para distribución (D-STATCOM, *Distribution Static Power Compensator*) es un dispositivo para la compensación de potencia reactiva en redes eléctricas de distribución que tiene ventajas sobre los capacitores convencionales debido a que evita resonancias de potencia y pueden} realizar una compensación continua, alcanzando factores de potencia cercanos a la unidad. Este artículo describe la implementación de un D-STATCOM para compensación reactiva en redes de distribución, haciendo una rigurosa explicación de cada uno de sus componentes. Se desarrolló un inversor trifásico de seis pulsos con dos niveles. Se describe completamente la implementación del hardware de las diferentes etapas (sensores, conmutación de potencia, elementos pasivos y procesador). El firmware que permite la operación del D-STATCOM se implementó en un DSP TMS3202F (Texas Instruments) con un enfoque modular. La correcta operación del prototipo de D-STATCOM se validó con resultados experimentales. Resultados mostraron una apropiada corrección del factor de potencia, reducción de la corriente demandada por la red eléctrica y un correcto funcionamiento del sistema de control, algoritmos y hardware.**

***Palabras claves*— DSP, D-STATCOM, electrónica de potencia, microcontroladores, procesamiento digital.**

This manuscript was sent on May 2, 2019 and accepted on December 17, 2019.

Grupo de Investigación en Manejo Eficiente de la Energía (GIMEL), Departamento de Ingeniería Eléctrica, Facultad de Ingeniería, Universidad de Antioquia, Calle 67 No 53-108, Medellín, Colombia.

S. Benavides-Cordoba, Facultad de Ingeniería, Universidad de Antioquia, Grupo de Investigación en Manejo Eficiente de la Energía (GIMEL), santiago.benavides@udea.edu.co.

J.R. Ortiz-Castrillón, Facultad de Ingeniería, Universidad de Antioquia, Grupo de Investigación en Manejo Eficiente de la Energía (GIMEL), jrobinson.ortiz@udea.edu.co.

N. Muñoz-Galeano, Facultad de Ingeniería, Universidad de Antioquia, Grupo de Investigación en Manejo Eficiente de la Energía (GIMEL), nicolas.munoz@udea.edu.co.

J.B. Cano-Quintero, Facultad de Ingeniería, Universidad de Antioquia, Grupo de Investigación en Manejo Eficiente de la Energía (GIMEL), bernardo.cano@udea.edu.co.

J.M. López-Lezama, Facultad de Ingeniería, Universidad de Antioquia, Grupo de Investigación en Manejo Eficiente de la Energía (GIMEL), jmaria.lopez@udea.edu.co.

I. Introduction

Reactive energy is mainly associated with the operation of electric devices such as transformers in power systems and motors in industrial applications [1]. Reactive energy is a bi-directional interchange between the load and the source in power systems causing power losses, reduction in the effective network capacity and deterioration of power quality [2]. Therefore, reactive energy must be compensated, minimizing its circulation in the power system. Many industrialized countries have implemented regulation that penalizes the excessive use of reactive consumption due to the over cost that it causes in distribution and transmission networks [3], [4].

An alternative to reactive power compensation is the use of capacitor banks. These are devices that are composed of switching capacitors, so compensation is made in a discrete way being useful in systems with variable loads. The continuous change in the topologies of the load and power network causes resonance problems when capacitor banks are installed, implying mal-functioning of the power network due to the presence of over voltages and currents [5]. These problems can be solved using controlled power electronic devices [6], [7], [8].

D-STATCOM is a promissory power electronic device to reactive power compensation. It is connected in parallel with

the load and can operate in a continuous way, reaching a power factor near the unity and avoiding operative problems. The most common topologies for D-STATCOM are multi-pulse and multi-level [7], [9]. Multi-level topology has more than six switches, each branch has three or more switches depending on the voltage level, which requires complex control schemes and higher costs [10]–[15]. Meanwhile, multi-pulse topology has six switches [16], two switches by branch. This topology has the fewest switches for a three-phase inverter [7], [8], [17]. Due to its lower cost and simplicity of control, multi-pulse topology was chosen in this research.

This paper presents a description of the implementation of a D-STATCOM. Hardware implementation is illustrated, including design details in Printed Circuit Boards (PCB). PCB of sensors, power switching, passive elements, and processor are fully described. Also, the firmware that allows D-STATCOM operation is detailed and illustrated. Such firmware was implemented using a TMS3202F DSP (Texas Instruments) with a modular approach.

This paper is structured as follows: In Section II the fundaments of reactive power compensation and D-STATCOM operation are described; in Section III the D-STATCOM hardware development is presented; in Section IV the firmware modules are described; in section V results are presented showing the D-STATCOM operation; finally, the most relevant conclusions are presented in Section VI.

II. D-STATCOM Operation

Reactive power is an oscillating energy that bi-directionally flows between electrical grids and loads; however, many loads such as motors need reactive power in their operation; D-STATCOM can provide this reactive power improving energy quality of the power network. Fig. 1 illustrates reactive energy compensation provided by a D-STATCOM. In this case the grid, load and the D-STATCOM are in parallel, having the same voltage (grid voltage v_G); i_G, i_L, i_D are grid, load and D-STATCOM currents respectively.

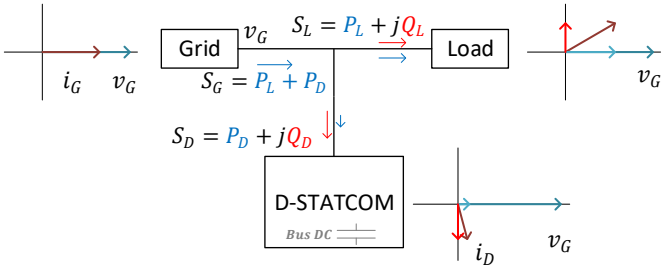


Fig. 1. D-STATCOM operation.

Using v_G as the reference in the horizontal axis, phasor diagrams are presented for each element in Fig. 1. Current i_L has a phase angle with respect to v_G, thus it can be decomposed into a horizontal (direct) projection (associated to load active power P_L) and a vertical (quadrature) projection (associated with load reactive power Q_L). During D-STATCOM operation, the quadrature component of i_D is controlled in order to be equal to the quadrature component of i_L with opposite sign. In this way, the grid current i_G has no quadrature component and thus no reactive power is interchanged with the grid.

In Fig. 1, D-STATCOM apparent power S_D is represented as the sum of an active power P_D and a reactive power Q_D. P_D corresponds to the power consumed by the D-STATCOM (including power losses) necessary for its operation. Q_D is used to compensate Q_L. Note that, grid apparent power (S_G) is equal to P_L plus P_D i.e. the grid only provides active power when D-STATCOM is in operation.

III. Hardware Description

Fig. 2 shows the D-STATCOM scheme and complementary elements for its operation. Fig. 2a presents D-STATCOM converter topology (two levels and six pulses) [7], [9]; while Fig. 2b shows additional electronic modules in charge of measurement and converter control.

D-STATCOM main component is the three-phase inverter (Voltage Source Converter, VSC), in charge of power flow regulation between the AC grid and the DC-bus (Fig. 2b). Such inverter consists of six insulated gate bipolar transistors (IGBTs) and is controlled by means of six switching signals: M^a, M^b, M^c for the upper transistors and $M^{a\prime}$, $M^{b\prime}$, $M^{c\prime}$ for the lower transistors.

The DC-bus is composed of capacitors C_1 and C_2 that are used for energy storing and guarantee a constant DC voltage for three phase inverter operation. Two stabilization resistors, in parallel with each capacitor, are used to minimize capacitor voltage unbalances due to neutral currents [18]. Also, to limit start-up currents when the DC-bus is discharged, a pre-charge circuit was added between the inverter and bus [17]. The pre-charge circuit consists of a series resistor that is short-circuited once the DC-bus has reached a pre-set voltage.

Three-phase grid connection is achieved by using a set of coupling inductances (L_a, L_b and L_c). Coupling inductances function is to filter high frequency components of output D-STATCOM currents (i_D^a ,i_D^b, i_D^c). Also, for safety and practical reasons, a series connection relays (C_e) are used to D-STATCOM disconnection.

The following sensors were implemented. Current sensors were used to measure D-STATCOM output currents (i_D^a ,i_D^b, i_D^c that are indicated as the vector i_D^{abc}) and load currents (i_L^a ,i_L^b, i_L^c that are indicated as the vector i_L^{abc}). Voltage sensors measure DC-bus voltage (v_{DC}) and three-phase grid voltages (v_G^{abc}). Sensor implementation and signal conditioning where implemented in the Current and Voltage Measurement PCBs (Fig. 2b.).

Sampling, calculations, control algorithms, control signal generation (M^{abc} and $M^{abc\prime}$) and communications are carried out by a microcontroller. Microcontroller PCB (Fig. 2b.) contains all the associated necessary circuitry for the correct microcontroller operation.

Table I summarizes the main specifications for the developed D-STATCOM. The next subsections describe in more depth the implementation of the different hardware blocks.

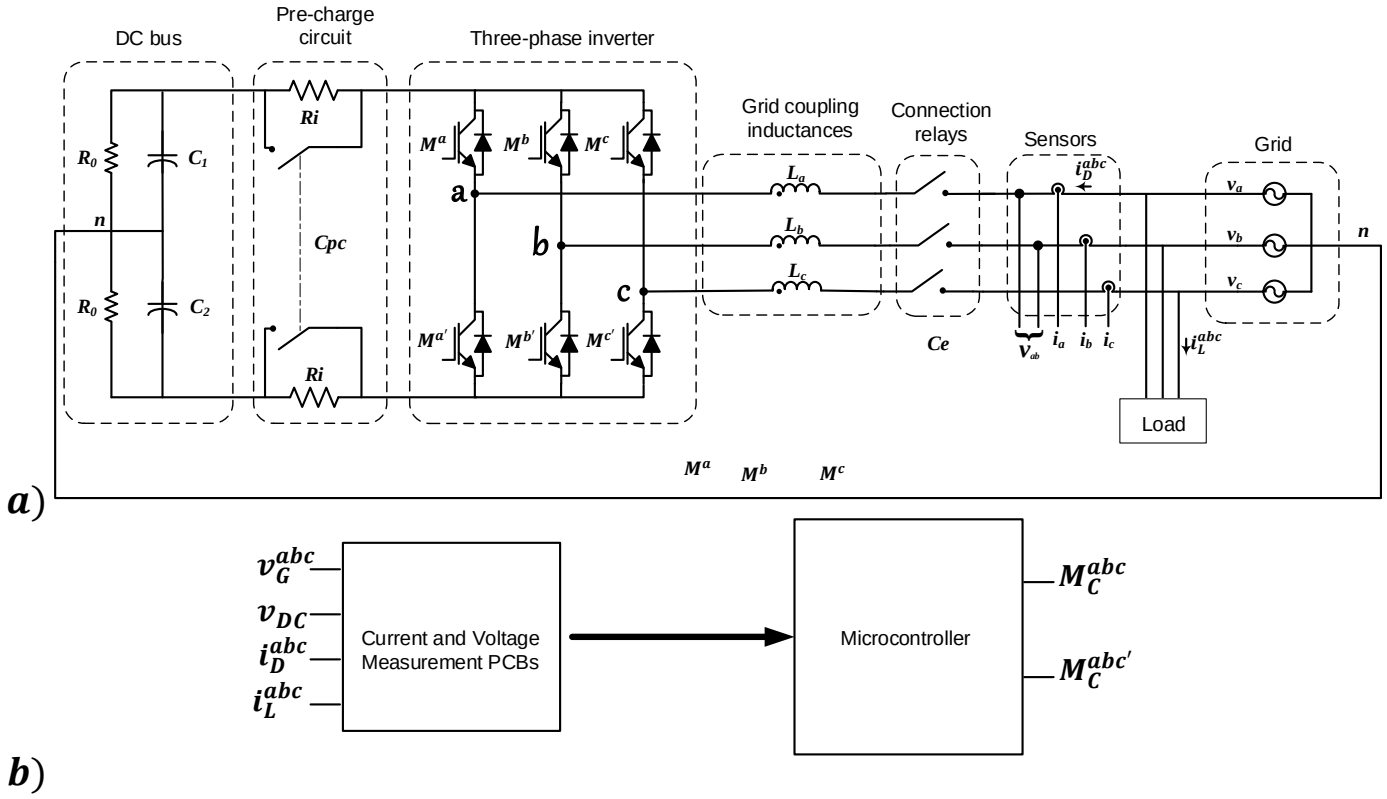


Fig. 2. D-STATCOM scheme and PCBs.

TABLE I
D-STATCOM CHARACTERISTICS

Characteristic	Value
Power	337.611 VA
Voltage	44 Vrms (transformer coupled to 220V grid)
Current	4.43 Arms
DC bus Voltage	283 Vdc
Coupling inductances	14 mH
Capacitors	2200 uF
Power factor correction	Inductive and capacitive

A. PCB for VSC

Fig. 3 presents the PCB implemented for the VSC and gate drivers. This PCB has three main stages: 1) VSC implementation, 2) Bootstrap capacitor implementation and 3) optocouplers implementation.

First stage, VSC implementation: The VSC was built with an Integrated Power Hybrid IC with internal shunt Resistor (IRAM136-3063B). This module has six power switches (IGBT) with anti-parallel diodes. Maximum operation current is 15 Amp (100ºC) while collector-emitter voltage is up to 600 Volts. Module includes gate-drivers for appropriated IGBT switching, allowing its control by means of 5V digital signals.

Second stage, Bootstrap capacitor implementation: Bootstrap capacitors are used to adequate the voltage signal for upper switches of VSC.

Third stage, optocouplers implementation: six optocouplers were used for isolation between the control system (microcontroller) and the VSC.

Finally, this PCB has a common connector for switching signals generated from the microcontroller ($M_C^{abc}, M_C^{abc\prime}$), terminals for bus DC connection and terminals for the VSC output.

To guarantee safety, durability and scalability, this PCB was designed taking into account the recommendations from IPC standard 2152 [19] for route sizing with respect to maximum current and IPC standard 2221 [20] and for clearance with respect to maximum voltage. These recommendations were also applied to the rest of PCBs developed.

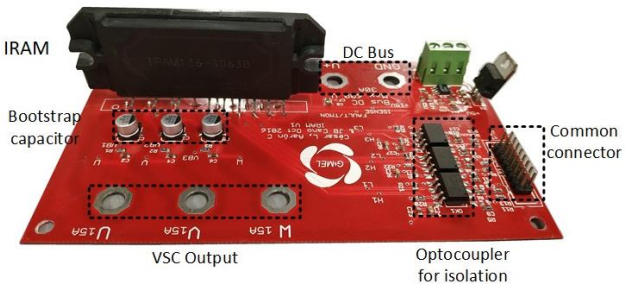


Fig. 3. PCB IRAM136-3063B and Gate Drivers.

B. *Current and Voltage Measurement PCBs*

Voltage measurement (v_{DC}, v_G^{abc}) and current measurement (i_D^{abc}, i_L^{abc}) were implemented in independent PCBs. Fig. 4 presents the voltage measurement PCB. This PCB is based on the AMC1200 isolation amplifier, allowing measurements up to 1000 Volts. AMC1200 is powered trough an isolated DC-DC power source. AMC1200 output is filtered through an active analog filter using the Sallen-Key topology. Analog signals from this PCB are in the range of 0 to 3.5V and are carried out to the microcontroller PCB through a common connector.

Voltage PCB can measure up to four different signals, thus a single card is enough for D-STATCOM requirements (v_{DC}, v_G^{abc})

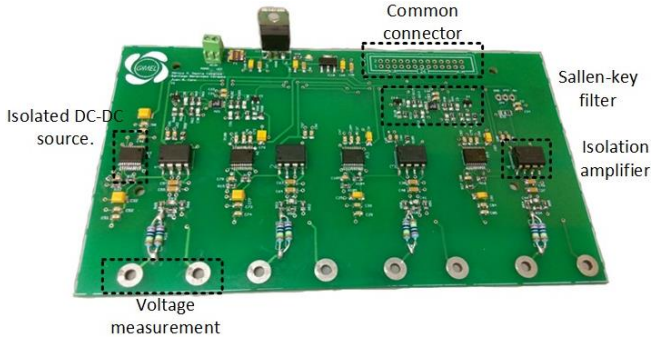


Fig. 4. Voltage measurement PCB.

Fig. 5 presents the current measurement PCB. This PCB has three current inputs and is based on the ACS174 hall effect sensor. ACS174 provides an isolated voltage output proportional to the sensed current, in the range of 0-5V. Signal conditioning is completed by a Sallen-Key filtering and attenuation to 0-3.5V range. Two PCBs are used, first for D-STATCOM currents measurement (i_D^{abc}) and second for load currents measurement (i_L^{abc}).

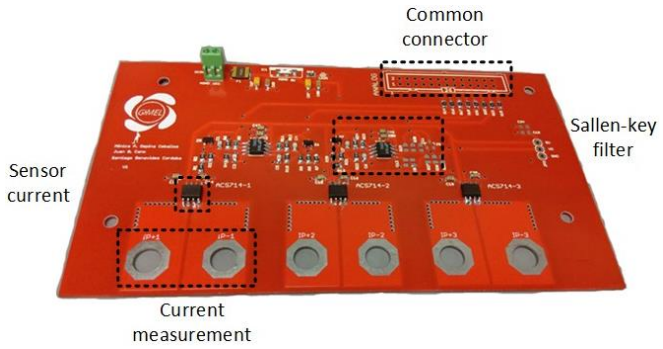


Fig. 5. Current measurement PCB.

C. *Passive elements*

DC-Bus and coupling inductors define limits for D-STATCOM compensation. In this subsection their sizing is detailed.

Coupling inductor sizing: inductor designing is done based on current signal geometry according to [21], [22]. Equation 1 presents the inductor value L, where Δi_L is the current ripple, f_{sw} is the switching frequency and n is the number of inverter levels. In this way, the selected coupling inductance for each phase is $L = 14\,mH$ (Fig. 6) in order to filter the current signal given by the IGBT module (grid coupling inductances in Fig. 2).

$$L = \frac{1}{n} \cdot \frac{v_{DC}}{\Delta i_L \cdot f_{sw}} \tag{1}$$

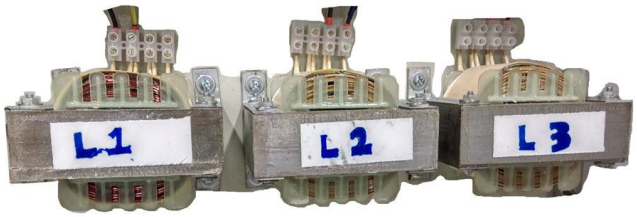


Fig. 6. Inductors for grid coupling.

DC bus sizing: capacitance value is defined by means of (2) from [21], [23]. Where $v_{out-peak}$ is the output voltage peak, i_{n-peak} is the neutral current peak, f_G is the grid frequency and Δv_c is the voltage ripple. In this case, D-STATCOM has 4 capacitors (split DC-Bus) of $2200\,\mu f$ (commercial value). In addition, 2 resistances of 30 kΩ are used to regulate the DC-Bus charge (pre-charge circuit in Fig. 2).

$$C = \frac{v_{out-peak} \cdot i_{n-peak}}{4\pi \cdot f_G \cdot v_{DC} \cdot \Delta v_c} \tag{2}$$

D. *Microcontroller*

D-STATCOM is a power electronics device that needs data measurement, serial communication, PI (Proportional Integral) controller and high-speed processing. Therefore, a microcontroller with DSP is necessary. In this case, the D-STATCOM controller was developed using a microcontroller TMS320F28335 (specialized in power electronics [24], [25]). Fig. 7 presents the PCB designed and implemented for the microcontroller. This PCB has 4 main stages:

First stage, microcontroller: this is a microcontroller DSP TMS320F28335 manufacturer by Texas Instruments. TMS320F family is focus on power electronics applications.

Second stage, common PWM terminals: these terminals are used to control the VSC.

Third stage, common measurement terminals: these terminals are used to receive measures from sensor PCBs.

Fourth stage, Serial Communication: these terminals are used to do an interface between microcontroller and users by means of USB port (SCI-USB).

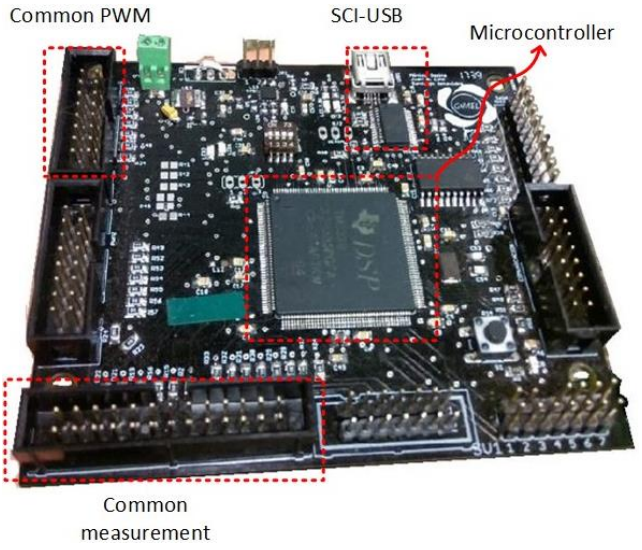


Fig. 7. PCB for microcontroller TMS320F28335.

IV. Firmware Description

This section describes the firmware that was implemented in the DSP TMS320F28335. TMS320F family manufacturer (Texas Instruments) provides specialized libraries in motor control [26], frequency analysis response [27] and photo-voltaic solar energy [28]. Also, the supplier provides detailed libraries with explanation of microcontroller peripheral programing for controlling power switches [29].

Math operations in a control system imply complex processing operations, which must be executed in a period of time shorter than the sampling period of the system. For this reason, it is convenient to use a microcontroller with floating-point (programmed for DSP) and fixed-point libraries in order to execute faster numeric calculations.

The DSP has an Arithmetic Logic Unit (ALU) module that is used to support the processor with complex math operations. Fixed-point libraries are codes to perform high speed math operations. Table II shows some functions for math operations of TMS320F family.

TABLE II
Functions of Fixed-Point and Floating-Point Libraries

Functions	Fixed-point	Floating-point
Complex FFT	6	1
Real FFT	8	2
Inverse Fourier Transform	1	0
Vector operations	7	0
Statics using vector	3	0
Infinite Impulse Response (IIR)	0	2
Design filter examples	0	4

Fig. 8 shows the main functions that TMS320F28335 executes for D-STATCOM operation. Voltages and currents digitalization is accomplished by using the ADC (Analog to Digital Converter) peripheral. Activation of the VSC IGBTS is accomplished using the PWM (Pulse Width Modulation) peripheral [30]. SCI (Serial Communications Interface) peripheral is used for communications while GPIO (General Purpose Input Output) peripheral is used for contactors activation (grid connection and pre-charge circuit).

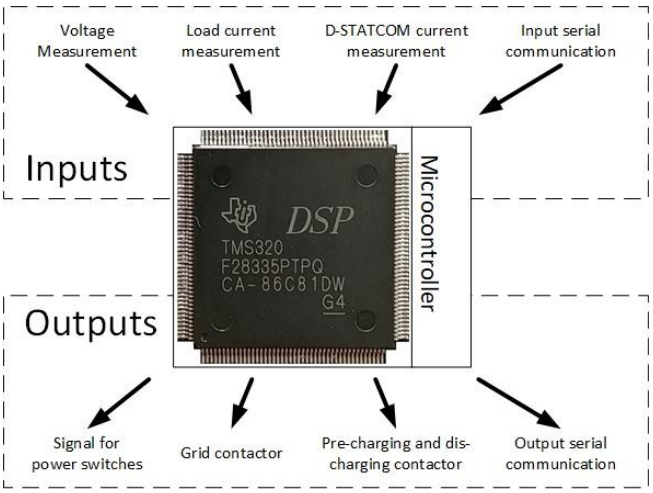


Fig. 8. Peripheral used in D-STATCOM development.

In order to control the microcontroller peripherals, a set of firmware modules were developed. These modules are shown in Fig. 9 and are described in the next subsections.

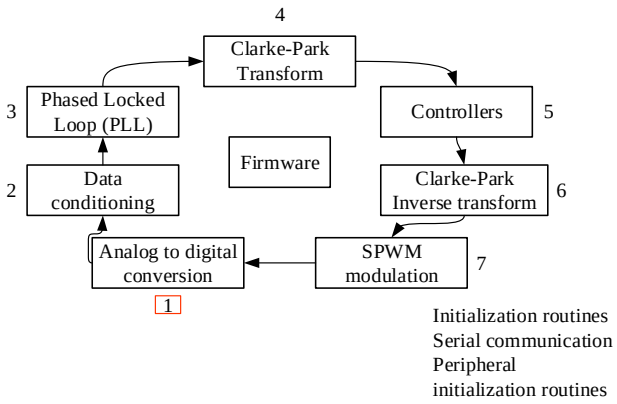


Fig. 9. D-STATCOM operation routines.

A. Analog to digital conversion and data conditioning

Control process initiates by measuring all voltage and current signals of the system (i_D^{abc}, i_L^{abc},v_{DC}, v_G^{abc}). TMS320F ADC was used. ADC resolution is 12 bits and sampling frequency is 20 kHz. Data conditioning consists of ADC data scaling, that permits to convert binary data to engineering units through an offset correction and a gain factor.

B. Phase-Locked Loop (PLL)

A phase-locked is a control system which permits the generation of signal whose output is related to the phase of an input signal. For power electronic devices, PLL is used to synchronize the voltages and currents of the system with a reference. In this case, the signal which is the reference of the system is the grid voltage of phase a (v_G^a). PLL was implemented using the library C28x Solar library [20], PLL algorithm is updated at every ADC sampling.

C. Clarke-Park transform

Clarke-Park transform changes three-phase AC signals into DC signals referenced to a rotational frame (dq0 frame) [31], [32]. It allows the representation of all phase currents in its direct and quadrature components using as reference the voltage v_c^a. This transform gives information about active power related to the direct current component and also reactive power related to the quadrature current component. Clarke-Park transform is performed by a sequence of instantaneous matrix operations that is performed at the same ADC sampling frequency. This transform comes from solar library [28] and uses the voltage and current data sampled from ADC and the phase angle determined by PLL. Using this transformation, D-STATCOM currents in dq0 frame (i_D^{dq0}) are obtained from i_D^{abc}, and load currents in dq0 frame (i_L^{dq0}) are obtained from i_L^{abc}.

D. D-STATCOM Controllers

D-STATCOM controllers generate control signals for IGBT power module. Cascade control and closed loop control are used to compensate reactive power. Fig. 10 shows the D-STATCOM control schemes: Fig. 10a presents the DC voltage control loop and Fig. 10b presents reactive current control loop.

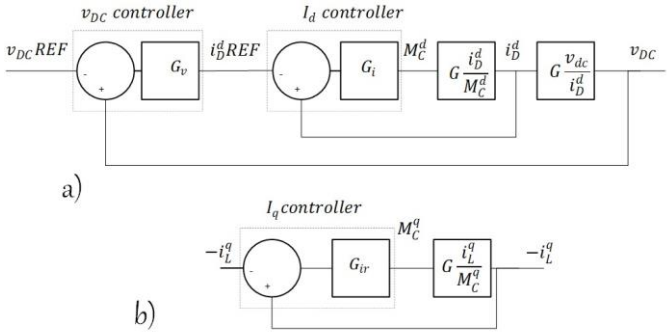


Fig. 10. D-STATCOM controller system.

DC voltage is controlled by absorbing or delivering active power from the grid (Fig. 10a). The input to the v_{DC} controller (G_v) is the error signal between the set point ($v_{DC}REF$) and sensed v_{DC}, and its output is the direct current component set point (i_D^dREF). In this way, G_v controller determines the amount of i_D^d (that is related to active power) required to keep v_{DC} at its desired level. Direct current controller (G_i) function is to keep the i_D^d value fixed at the level i_D^dREF by modifying the direct modulation output (M_C^d) that defines IGBT switching. Blocks Gi_D^d/M^d and Gv_{dc}/i_D^d represent the transfer functions for the D-STATCOM model [18].

Fig. 10b presents the reactive currents of the control loop. Note that, in this case, a voltage controller is not necessary. This is due to the oscillating nature of the reactive power, which does not affect the v_{DC} average value but affects its ripple. The set point for the closed loop controller (G_{ir}) is the negative value of the load quadrature current ($-i_L^q$). In this way, this controller guarantees that the D-STATCOM system behaves as a controlled current source; that is, always equal to the reactive current of the load. The output from this controller is the quadrature modulation (M_C^q) that defines the IGBT switching.

All controllers use PI (proportional integrative) control law and were implemented using Texas instruments libraries and tuned using the methods described in [17]. Sampling rate for current controllers (G_i , G_{ir}) is 4KHz, and for DC voltage controller (G_v) is 800Hz.

E. Inverse Clarke-Park transformation

Controller outputs (M_C^d and M_C^q) are related to dq0 frame. M_C^{dq} must be converted to time domain using inverse Clarke-Park transformation. Inverse Clarke-Park transformation provides three sinusoidal signals (M_C^{abc}) with a difference of 120° between phases which will be used as reference in the SPWM (Sinusoidal Pulse Width Modulation). For inverse transformation, it is assumed that $M_C^0 = 0$, implying that the D-STATCOM output currents are balanced.

F. SPWM modulation

SPWM generates switching signals for the IGBT modules that are based on the results obtained from the inverse Clarke-Park transformation. SPWM modulation is carried out by using the microcontroller enhanced Pulse Width Modulation (ePWM) peripheral.

Fig. 11 shows a bipolar modulation for an arbitrary phase. Modulation consists in the comparison between a sinusoidal signal (reference signal) and a triangular signal (carrier signal). In this implementation, the reference signal is M_C^{abz} while the triangular signal is generated by a digital counter in the ePWM peripheral.

Reference and Carrier signals are continuously compared. Every time that the reference signal is higher than the carrier signal, the upper IGBT is activated and the lower IGBT is deactivated. Instead, when reference signal is lower than carrier signal, the upper IGBT for that phase is deactivated and the lower IGBT is activated. Note that this process is executed for the three phases, providing the six switching signals of Fig. 2a (M^{abc} for upper IGBT and $M^{abc\prime}$ for lower IGBT).

Also, ePWM peripheral provides dead time functionalities, which avoid VSC destruction due to simultaneous activation of upper and lower IGBTs of the same phase.

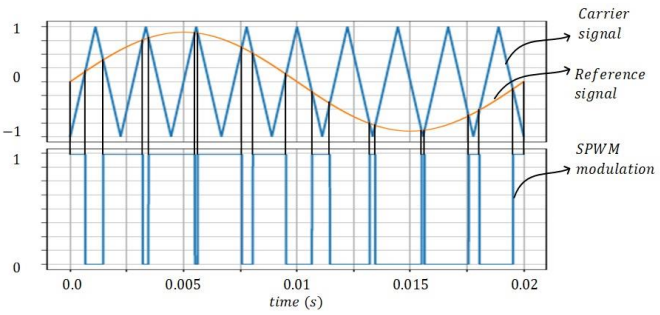


Fig. 11. Bipolar SPWM modulation.

G. Initialization routine

After a power on condition, and before system operation, a series of initialization steps must be carried on in order to

guarantee a proper initial condition for controllers and a safe start operation.

Fig. 12 shows the algorithm for D-STATCOM initialization: 1) Initial conditions: Initially, grid connection contactor is opened while microcontroller initializes all its peripherals. 2) DC bus discharge: Microcontroller verifies that the DC bus is discharged before initiating operation. 3) Delay for DC level measurement: During a given period, measurements of all sensors (current and voltage) are captured for offset compensation. 4) Grid connection: Grid contactor is closed. 5) Capacitor pre-charging routine: DC voltage starts to increase, but DC-bus current is limited by the two pre-charging resistors, once voltage reaches a given threshold, pre-charging resistors are short-circuited using pre-charging contactors. 6) Controllers initialization: Control loop described in previous sections is started.

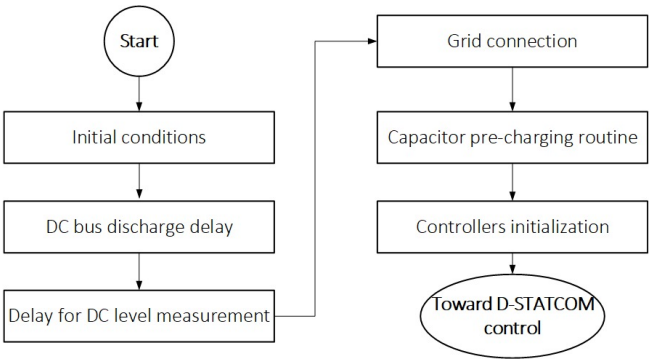


Fig. 12. Initialization algorithm

H. *Serial communications.*

This firmware module controls the SCI peripheral which using a FTDI232 interface provides USB communication for the D-STATCOM. This module consists of a finite state machine that receives request of information from user and responds sending data.

Part of the microcontroller's memory is reserved for saving data of load currents (i_L^{abc}), D-STATCOM current (i_D^{abc}), grid voltage (v_g^{abc}), dq0 transformations (i_L^{dq0}, i_D^{dq0}), control variables (M_C^{dq}). Memory contents are serially transferred under user request. This mechanism helps to diagnose the system operation and was used to obtain some of the results for the next section.

V. Results

In this section, the main results obtained from the D-STACOM prototype are presented. Subsections present results for selected individual modules and finally the D-STATCOM operation is shown.

Fig. 13 shows the implemented D-STATCOM and its main components: 1) Coupling contactor for grid connection, breakers and fuses for protection of PCBs and voltage sources. 2) Voltage measurement PCB. 3) microcontroller PCB. 4) Current measurement PCB. 5) Pre-charge contactor. 6) Pre-charge resistances. 7) PCB of VSC IRAM136-3063B. 8) Relays for actioning contactors. 9) DC bus capacitors. 10) Inductors for grid coupling.

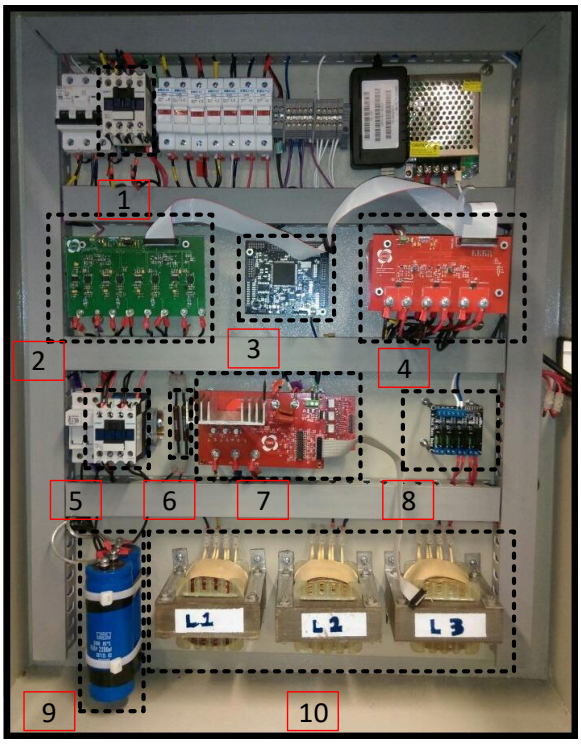


Fig. 13. D-STATCOM.

A. *Sensors, Analog to digital conversion and data conditiong*

In this section, a validation of the measurement systems is shown. Table III presents the measured voltage by means of a scope GW INSTEK GDS-2240A and with the sensor voltage PCB. Fig. 14 presents a plot and linear regression of data from Table III; it is shown the linearity of sensor for voltage measurement with a $R^2 = 0.996$; this property allows the sensor calibration using any calibration device.

TABLE III
Measurement of Voltage Sensor

Input voltage measured (rms)	Microcontroller voltage (rms)
60.10	0.6717
50.00	0.5727
40.20	0.4737
30.40	0.3747
20.20	0.2616
10.50	0.1626

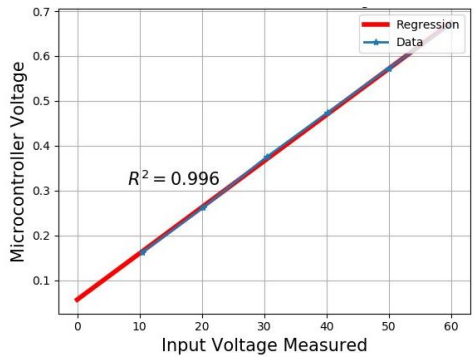


Fig. 14. Sensor linearity.

The same procedure was applied to all current and voltage sensors, providing reliable measurements. Fig. 15 shows a sinusoidal signal from the electrical grid that is captured by the ADC and its respective binary vector.

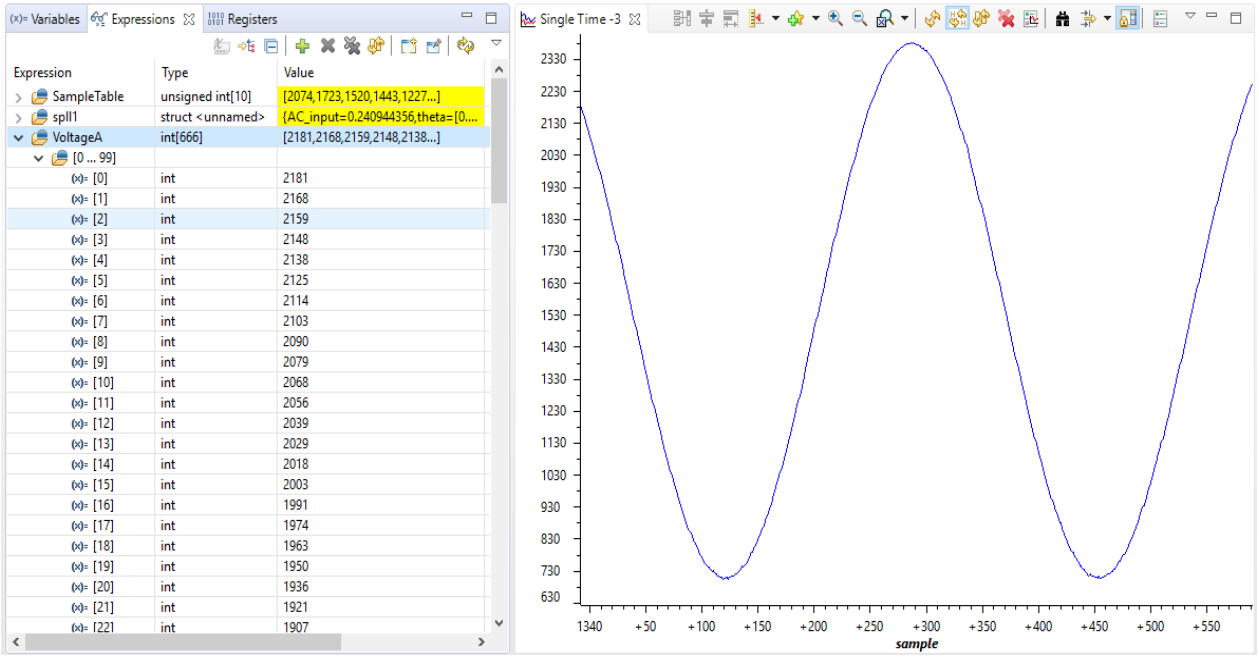


Fig. 15. Voltage measurement of phase A.

B. *Phased locked loop (PLL)*

Fig. 16 shows the PLL algorithm behavior (PLL algorithm following the grid signal). In this figure, the red sinusoidal signal corresponds to the grid voltage that is measured trough sensor PCB, sampled by ADC and entered to PLL algorithm. The blue signal is a digital signal generated by the microcontroller. It is programed to change state every time that the PLL algorithm predicts a zero cross of the grid signal. The PLL works correctly when the square signal changes its state with sinusoidal signal zero crossing. Fig. 15 presents three stages: 1) microcontroller off, blue signal is off; 2) microcontroller turns on and PLL start to search for grid synchronization; and 3) PLL is synchronized with the grid.

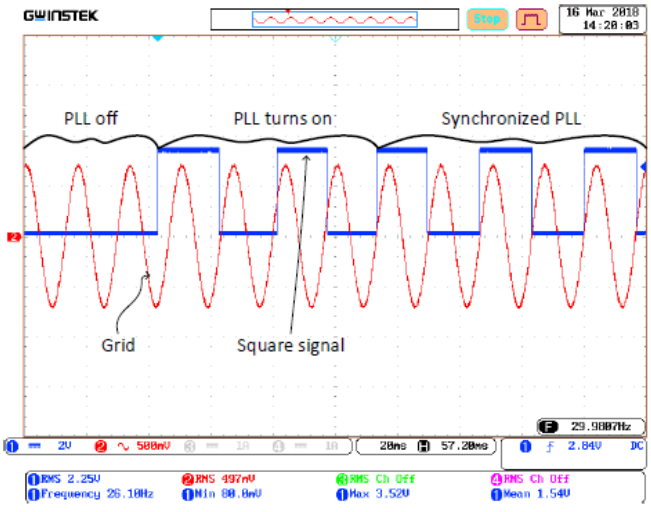


Fig. 16. PLL behavior.

C. *Clarke-Park transform*

Fig. 17 shows the Clarke-Park transform done by the TMS320F28335 microcontroller. Fig. 17a shows the time domain of the three-phase D-STATCOM currents in open loop without load; currents (i_D^{abc}) are shown in solid blue (i_D^a) orange (i_D^b) and green (i_D^b) colors, also grid phase (v_G^a) voltage of phase A is shown in dotted black (only for the reference phase). In figure 17a, i_D^a is leading to v_G^a, it means that D-STATCOM has a capacitor behavior (it provides reactive power).

Fig. 17b shows dq0 transformation of current signals using the algorithm described in previous sections. The blue signal represents current direct component (i_D^d) associated to the D-STATCOM active power, the orange signal represents current quadrature component (i_D^q) associated to positive reactive power and finally, the green signal represents zero component (i_D^0) associated with unbalances between phases.

Note that the time domain signals exhibit unbalances due to load imperfections. This explains the presence of i_D^0 component in its dq0 transformation.

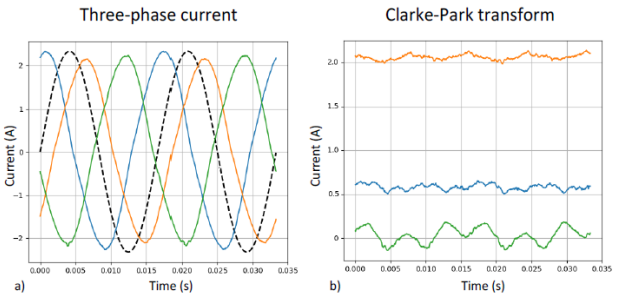


Fig. 17. Park transform done by microcontroller TMS320F28335.

D. SPWM modulation

Fig. 18 shows microcontroller SPWM modulation at minimum and maximum values of reference signal.

Reference signal (M_C^a) is shown in green and SPWM modulation is shown in red. Note that when the reference signal is at its minimum, the modulation signal is at low level most of the time (i.e. lower IGBT activated). Instead, when the reference signal is at its maximum, the modulation signal is at its maximum value (i.e. upper IGBT activated) most of the time.

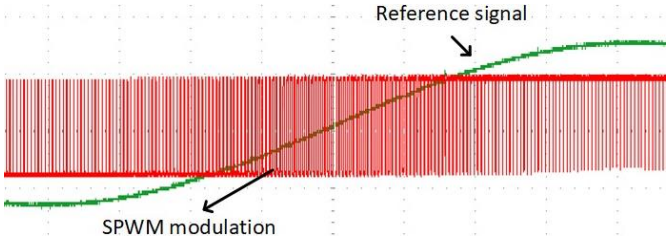


Fig. 18. SPWM modulation implemented.

E. D-STATCOM operation

In this subsection, operation of D-STATCOM as a complete system is evaluated. Inductive and capacitive loads where connected to the grid and D-STATCOM capacity to compensate reactive power was observed.

Fig. 19 shows the D-STATCOM behavior operating as a capacitor taken from oscilloscope. In Fig. 19a, it is observed that currents (4.43 Arms) from phases A (upper graphic), B (middle graphic) and C (low graphic) are leading respect to grid voltage (44 Vrms). A phasor diagram is presented in Fig.19b; this figure shows a D-STATCOM angle of 81.63° (close to 90° due to active power losses) with respect to grid voltage. Fig. 19c presents the harmonics from current signal of phase A, where the THD is lower than 5%.

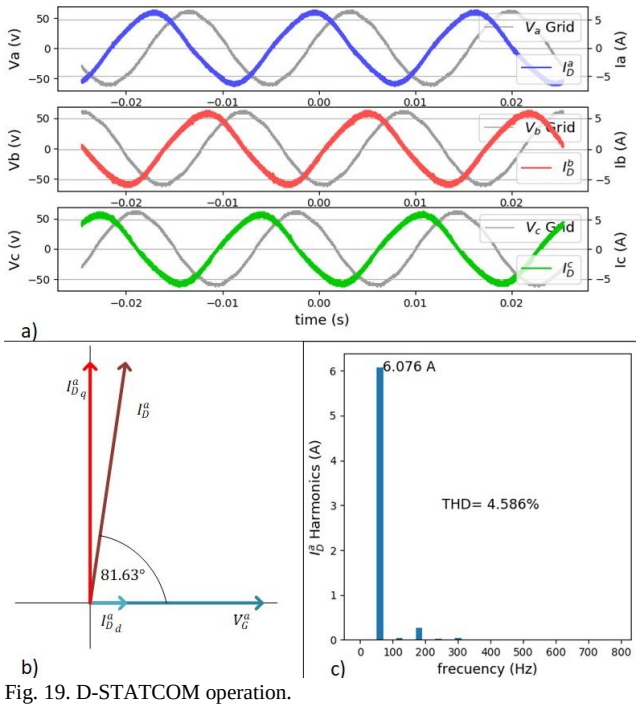


Fig. 19. D-STATCOM operation.

First, a resistive-inductive load was tested. Fig. 20 shows grid current signals in time domain before and after D-STATCOM operation, phase current A is blue, B is red and C is green, also each plot reproduces in gray the respective grid phase voltage in order to have phase references. Note that Fig 20 plots are divided in two parts: the left side shows grid currents without D-STATCOM operation and the right side with D-STATCOM operation. The transient condition due to STATCOM start is omitted, showing only steady state.

It can be seen that after D-STATCOM operation, the grid currents and voltages appear to be on phase. This can be verified in the phasor diagrams shown in Fig. 20a and Fig. 20b. Before operation, the grid current has a -33.02º angle against voltage, after starting the operation of the D-STATCOM, the angle was reduced to 5.11º. Considering power factor, this corresponds to a correction from 0.83 to 0.99. Note also that the grid current magnitude was decreased.

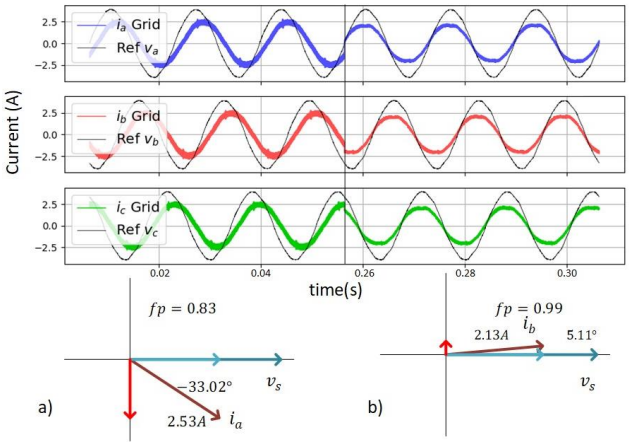


Fig. 20. D-STATCOM operation with resistive-inductive load.

Fig. 21 presents the operation results when the D-STATCOM compensates a capacitive load. Such load is nonlinear, demanding reactive power and injecting harmonics to the electrical grid. Fig. 21a shows measurements before D-STATCOM operation. In this state, load has a power factor of 0.049 and the phasor diagram shows a load current of 2.04 Amp in quadrature with v_s, i.e. load mainly demands reactive energy. Fig.21b shows measurements after D-STATCOM operation. Power factor is increased up to 0.99 remaining only the harmonic distortion caused by the load. In consequence, the current demanded from the electrical grid decreased up to 0.49 Amp

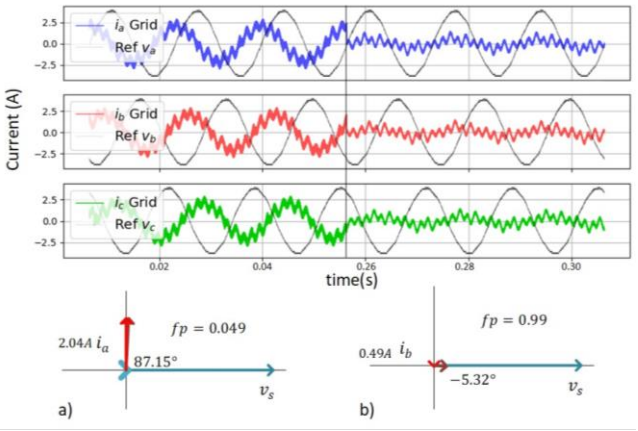


Fig. 21. D-STATCOM operation with capacitive load.

VI. Conclusions

In this paper, a description of hardware and firmware development for a D-STATCOM was presented; D-STATCOM main function is reactive power compensation. The implemented prototype includes voltage and current measurement, signal processing, control algorithms, switching and associated hardware. Most relevant prototype parts were described and its functionality was verified.

The D-STATCOM operation results showed power factor correction, reduction in current demanded to electrical grid and correct behavior of control system, algorithms and hardware.

The D-STATCOM prototype demonstrated that it is technically possible to replace traditional reactive power compensation techniques (as capacitive banks) in distribution networks. It also allows a precise control of the reactive power; furthermore, digital electronics devices can be remotely monitored, enhancing diagnostics and maintenance.

This prototype becomes a research platform for testing different control schemes, and even implementation of harmonics and unbalances compensation. Also, due to its modular conception, the D-STATCOM can be used in AC systems and power electronics practical teaching.

Acknowledgment

The authors gratefully acknowledge the financial support provided by the Colombia Scientific Program within the framework of the call Ecosistema Científico (Contract No. FP44842- 218-2018). Likewise, Universidad de Antioquia (Colombia) is acknowledged for the financial support through the "Sostenibilidad" program.

References

[1] J. H. Han, M. Y. Jang, G. B. Lee, B. S. Jang, and Y. A. Kwon, "Improved Performance of Sensorless Induction Motor Using Reactive Power," in *SICE Annual Conference 2007*, 2007, pp. 637–642. DOI: 10.1109/SICE.2007.4421060

[2] K. Bhattacharya and J. Zhong, "Reactive power as an ancillary service," *IEEE Trans. Power Syst.*, vol. 16, no. 2, pp. 294–300, May 2001. DOI:10.1109/59.918301

[3] K. Abinaya, D. Danalakshmi, and S. Kannan, "Cost analysis of reactive power using marginal cost theory in electricity markets," in *2014 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2014]*, 2014, pp. 79–83. DOI:10.1109/ICCPCT.2014.7055055

[4] H. Moreno, S. Plumel, and P. Bastard, "Assessing the value of reactive power service using OPF of reactive power," in *2005 IEEE Russia Power Tech*, 2005, pp. 1–6. DOI:10.1109/PTC.2005.4524430

[5] H. L. Santos, J. O. S. Paulino, W. C. Boaventura, L. M. R. Baccarini, and M. L. Murta, "Harmonic Distortion Influence on Grounded Wye Shunt Capacitor Banks Protection: Experimental Results," *IEEE Trans. Power Deliv.*, vol. 28, no. 3, pp. 1289–1296, Jul. 2013. DOI:10.1109/TPWRD.2013.2253805

[6] E. H. Ismail, "Bridgeless SEPIC Rectifier With Unity Power Factor and Reduced Conduction Losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009. DOI: 10.1109/TIE.2008.2007552

[7] O. K. Shinde and V. R. S. V. B. Pulavarthi, "STATCOM converters and control: A review," in *2017 International Conference on Data Management, Analytics and Innovation (ICDMAI)*, 2017, pp. 145–151. DOI: 10.1109/ICDMAI.2017.8073500

[8] J. Dixon, L. Moran, J. Rodriguez, and R. Domke, "Reactive Power Compensation Technologies: State-of-the-Art Review," *Proc. IEEE*, vol. 93, no. 12, pp. 2144–2164, Dec. 2005. DOI: 10.1109/JPROC.2005.859937

[9] P. Garcia-Gonzalez and A. Garcia-Cerrada, "Control system for a PWM-based STATCOM," *IEEE Trans. Power Deliv.*, vol. 15, no. 4, pp. 1252–1257, Oct. 2000. DOI: 10.1109/61.891511

[10] L. K. Haw, M. Dahidah, and N. Mariun, "Cascaded multilevel inverter based STATCOM with power factor correction feature," in *2011 IEEE Conference on Sustainable Utilization and Development in Engineering and Technology (STUDENT)*, 2011, pp. 1–7. DOI:10.1109/STUDENT.2011.6089317

[11] A. Mohammad and K. B. H., "Design and Evaluation of Solar Inverter for Different Power Factor Loads," *Energy Power Eng.*, vol. 2012, Sep. 2012. DOI:10.4236/epe.2012.45042

[12] F. R. U. Ramos, J. P. Ramírez, J. A. B. Jiménez, and L. J. H. Hernández, "Multi-level inverter connected to the grid with harmonic mitigation for photovoltaic power injection," in *2017 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC)*, 2017, pp. 1–6. DOI:10.1109/ROPEC.2017.8261662

[13] M. S. I. Tarek, A. Siam, M. Zia, and M. M. Rahman, "A Novel Five-Level Inverter Topology with Reactive Power Control for Grid-Connected PV System," in *2018 International Conference on Smart Grid and Clean Energy Technologies (ICSGCE)*, 2018, pp. 101–105. DOI: 10.1109/ICSGCE.2018.8556812

[14] P. Sotoodeh and R. D. Miller, "A single-phase 5-level inverter with FACTS capability using modular multi-level converter (MMC) topology," in *2013 International Electric Machines Drives Conference*, 2013, pp. 1229–1234. DOI: 10.1109/IEMDC.2013.6556290

[15] R. A. Krishna and L. P. Suresh, "A brief review on multi level inverter topologies," in *2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT)*, 2016, pp. 1–6. DOI:10.1109/ICCPCT.2016.7530373

[16] B. Muruganantham, R. Gnanadass, and N. P. Padhy, "Reactive Power Reallocation in the Distribution System with DSTATCOM," *Energy Procedia*, vol. 117, pp. 485–492, Jun. 2017. DOI:10.1016/j.egypro.2017.05.174

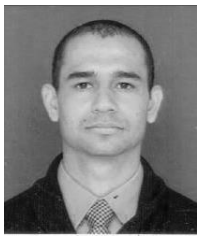
[17] S. B. Córdoba, J. R. O. C, J. B. C. Q, and N. M. G, "Consideraciones técnicas para la sintonización de los controladores de un D-STATCOM real a partir de un modelo simulado," *Av. Investig. En Ing.*, vol. 15, no. 1, pp. 256–270, Dec. 2018. DOI: 10.18041/1794-4953/avances.1.4738

[18] N. Mendalek, "Modeling and control of three-phase four-leg split-capacitor shunt active power filter," in *2009 International Conference on Advances in Computational Tools for Engineering Applications*, 2009, pp. 121–126. DOI: 10.1109/ACTEA.2009.5227933

[19] IPC, "IPC-2152 — Standard for Determining Current-carrying Capacity in Printed Board Design Released," 24-Sep-2009.

[20] IPC, "IPC-2221B: Generic Standard on Printed Board Design," 20-Nov-2012.

[21] W. C. Alves, L. M. F. Morais, and P. C. Cortizo, "Design of an Highly Efficient AC-DC-AC Three-Phase Converter Using SiC for UPS Applications," *Electronics*, vol. 7, no. 12, 2018. DOI:10.3390/electronics7120425
[22] "Grid Filter Design," in *Grid Converters for Photovoltaic and Wind Power Systems*, John Wiley & Sons, Ltd, 2010, pp. 289–312. ISBN: 9780470667057.
[23] M. E. Fraser, C. D. Manning, and B. M. Wells, "Transformerless four-wire PWM rectifier and its application in AC-DC-AC converters," *IEE Proc. - Electr. Power Appl.*, vol. 142, no. 6, pp. 410–416, Nov. 1995. DOI:10.1049/ip-epa:19952278
[24] J. Saavedra, J. Firacaitve, and C. Trujillo, "Development board based on the TMS320F28335 DSP for applications of power electronics," *Tecciencia*, vol. 10, no. 18, pp. 36–44, Jan. 2015. DOI:10.18180/tecciencia.2015.18.6
[25] G. E. M. Ruiz, N. Muñoz, and J. B. Cano, "Design methodologies and programmable devices used in power electronic converters — A survey," in *2015 IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA)*, 2015, pp. 1–6. DOI:10.1109/PEPQA.2015.7168214
[26] Texas Instruments Inc., "Digital Motor Control. Software Library: Target Independent Math Blocks." C2000 Systems and Applications, 2013.
[27] Texas Instruments Inc., "C2000 Software Frequency Response Analyzer (SFRA) Library & Compensation Designer. Module User's Guide," 2015. [Online]. Available: http://www.ti.com/lit/ug/spruhz5a/spruhz5a.pdf. [Accessed: 30-Aug-2018].
[28] Texas Instruments Inc., "C28x Solar Library. Module User's Guide." 2014.
[29] Texas Instruments Inc., "ControlSUITE for C2000 - Texas Instruments Wiki," 2018. [Online]. Available: http://processors.wiki.ti.com/index.php/ControlSUITE_for_C2000. [Accessed: 30-Aug-2018].
[30] Texas Instruments Inc., "TMS320F2833x, TMS320F2823x Digital Signal Controllers (DSCs). DataSheet," 2016. [Online]. Available: http://www.ti.com/lit/ds/symlink/tms320f28235.pdf. [Accessed: 31-Aug-2018].
[31] P. Szczesniak, Z. Fedyczak, and M. Klytta, "Modelling and analysis of a matrix-reactance frequency converter based on buck-boost topology by DQ0 transformation," in *2008 13th International Power Electronics and Motion Control Conference*, 2008, pp. 165–172. DOI:10.1109/EPEPEMC.2008.4635262
[32] L. Cociu, C. G. Haba, and V. R. Cociu, "Particularities of park transformation in special cases," in *2011 7th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, 2011, pp. 1–6.



Santiago Benavides-Cordoba (Bogotá, Colombia, 1990). He received a B. E. degree in Electric Engineering (UdeA-2016) and a master in engineering (UdeA-2018) in the energy management at University of Antioquia. He is member of the research group GIMEL. His research work is focused in power electronics.
ORCID: http://orcid.org/0000-0002-9207-866X

José R. Ortiz-Castrillón (Caldas, Colombia, 1989). He received a B. E. degree in Electric Engineering at the University of Antioquia (UdeA-2017). Currently, he is engineering master student in the energy management line of University of Antioquia (Colombia) and member of the research group GIMEL. His research work is focused in power electronics line and electrical storage systems.
ORCID: http://orcid.org/0000-0002-3794-0982

Nicolás Muñoz-Galeano (Medellín, Colombia, 1981). He received a B. E. degree in Electric Engineering at the University of Antioquia (UdeA-2004), and the Ph.D. degree in Electronics Engineering (UPVLC-2011). Since 2005 he has been professor of the Electric Engineering Department at the University of Antioquia (Colombia) and member of research group GIMEL. His research work is focused in power electronics design, control and electrical machines.
ORCID: http://orcid.org/0000-0003-1407-5559

Juan B. Cano-Quintero (Medellín, Colombia, 1986). He received a B. E. degree in Electronics Engineering at the University of Antioquia (Colombia-2008) and PhD degree on Sensor and Learning Systems at Tor Vergata University (Italy-2012). Since 2012 he is full-time professor at Electrical Engineering department at University of Antioquia. It's research interest are power electronics, sensor systems and solar energy.
ORCID: http://orcid.org/0000-0003-4767-1007

Jesús M. López-Lezama (Chinchiná, Colombia, 1978). He received the B.Sc. and M.Sc. degrees from the Universidad Nacional de Colombia in 2001 and 2006, respectively. He also received his Ph.D. degree at the Universidade Estadual Paulista (UNESP), SP, Brazil in 2011. Currently he is an associate Professor at Universidad de Antioquia, Medellín, Colombia. His major research interests are planning and operation of electrical power systems and distributed generation.
ORCID: http://orcid.org/0000-0001-6213-4133